# ADICHUNCHANAGIRI UNIVERSITY

**18EC32**

**Third Semester BE Degree Examination January 2020**

**(CBCS Scheme)**

Time: 3 Hours | Max Marks: 100 Marks

**Sub: ANALOG ELECTRONICS**

**Instructions:**
1. Answer five full questions
2. Choose one full question from each module
3. Your answer should be specific to the questions asked
4. Write the same question numbers as they appear in this question paper
5. Write Legibly.

## Module -1

| | | | |
|---|---|---|---|
| 1 | a | Define h-parameter. Draw the h-parameter model of a CE configuration. | 10 M |
| | b | Derive an expression for $I_B$, $I_C$ and $V_{CE}$ for voltage divider bias using exact analysis. | 10 M |

Or

| | | | |
|---|---|---|---|
| 2 | a | Derive an expression for Av, Zi, Zo for Emitter follower using re model | 10 M |
| | b | A voltage divider biased circuit has Rc=4KΩ, $R_E$=1.5KΩ, $R_1$=39KΩ, R2=3.9KΩ Vcc=18V and β=70. Find Ic,$V_{CE}$. | 10 M |

## Module -2

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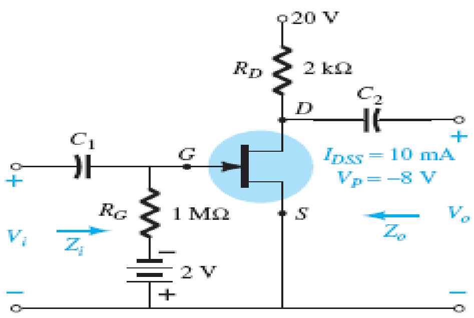
|---|---|---|---|
| 3 | a | Explain high frequency response of FET amplifier and derive an expression for cut off frequencies defined by input and output circuits. | 10 M |
| | b | Determine the lower cut off frequency for the FET amplifier using the following parameters $C_G$=0.01µF,$C_C$=0.5 µF,$C_S$=2 µF Rsig=10KΩ , $R_G$=1MΩ, $R_D$=4.7KΩ,Rs=1KΩ,$R_L$=2.2KΩ, $I_{DSS}$=8mA,Vp=-4v $r_{d=}$∞Ω,$V_{DD}$=20V,$V_{GSQ}$=-2V,$I_{DQ}$=2mA | 10 M |

Or

| | | | |
|---|---|---|---|
| 4 | a | Derive an expression for Zi and Zo, Av for self-bias configuration for JFET. | 10 M |
| | b | The fixed-bias configuration of FET amplifier had an operating point defined by $V_{GSQ}$ = -2 V and $I_{DQ}$ = 5.625 mA, with $I_{DSS}$ = 10 mA and VP = -8 V. The network is shown below with an applied signal Vi Yos=40µS. | 10 M |



## Module -3

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|---|---|---|---|---|
| 5 | a | Explain CS amplifier with necessary circuit and equations with and without source resistance | 12 | M |
| | b | From small signal operation of an amplifier derive an expression for DC bias point, signal current in Drain terminal ($i_D$), voltage gain and trans conductance | 08 | M |

Or

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|---|---|---|---|---|
| 6 | a | With neat diagram and small signal model of common drain amplifier prove that Avo=1,Gv=1 | 10 | M |
| | b | Explain the different types of internal capacitances in MOSFET and explain the gate capacitive effect. | 10 | M |

## Module -4

| | | | | |
|---|---|---|---|---|
| 7 | a | For a voltage series feedback amplifier topology. obtain an expression for Av, Rif and Rof also explain the practical feedback circuit using voltage series feedback. | 10 | M |
| | b | with neat circuit diagram explain the working of series resonant crystal oscillator.A crystal oscillator has L=0.334H, C=0.065pF,$C_M$=1pF,R=5.5KΩ calculate its series and parallel resonating frequency. | 10 | M |

Or

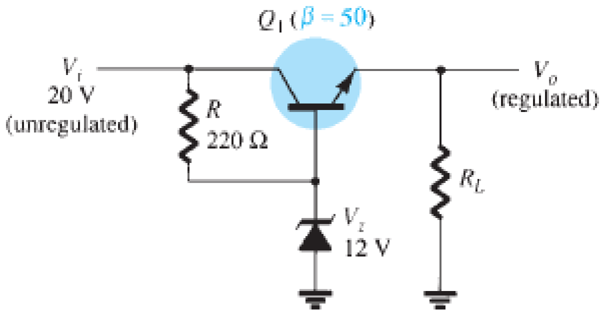
| | | | | |
|---|---|---|---|---|
| 8 | a | What are tuned oscillators? Explain the two types of tuned oscillators. | 10 | M |
| | b | Briefly explain Barkhausen criterion for oscillations and explain RC phase shift oscillator with necessary circuit and equations. | 10 | M |

## Module -5

| | | | | |
|---|---|---|---|---|
| 9 | a | Explain the working of class B push pull power amplifier. Derive an expression for its efficiency S T η=78.4% | 10 | M |
| | b | Derive an expression for second harmonic distortion in power amplifier using 3-point method. | 10 | M |

Or

| | | | | |
|---|---|---|---|---|
| 10 | a | With neat circuit diagram explain the operation of a series-fed class A power amplifier and prove that η=25%. | 10 | M |
| | b | Briefly explain the series voltage regulator. Calculate the output voltage and the Zener current in the regulator circuit of Figure shown below for $R_L$ = 1KΩ | 10 | M |

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